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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,471	01/29/2004	Takeshi Morita	2004_0135A	3718

513 7590 07/03/2006

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,471	MORITA, TAKESHI	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 5-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE and Amendment filed on May 9, 2006.

Claim Objections

Claim 9 is objected to because of the following informalities: Claim 9 contains the limitation of "said writing pattern" in line 9. It is assumed that "writing" is supposed to be "wiring." If that is the case, then the phrase "said wiring pattern" lacks antecedent basis in the claims. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 5-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takizawa (US 6,504,254 B2).

In re claim 1, Takizawa shows (figs. 1, 2, and 4b) a semiconductor device comprising: a semiconductor substrate (10) having a pattern forming region (containing wires 20a) and a pattern non-forming region (containing dummy patterns 34); a wiring pattern (20a) formed on said pattern forming region; a plurality of dummy patterns (34) formed on said pattern non-forming region, said plurality of dummy patterns being formed within a plurality of dummy areas (30), each of the dummy areas having a same

shape (hexagonal); an insulating film (40) formed on said wiring pattern and said plurality of dummy patterns); wherein the insulating film is smoothed by chemical mechanical polishing (col. 3, lines 63-67). Takizawa shows (fig. 4b) an alternate embodiment in which the each of said plurality of dummy patterns (30) has a plurality of line patterns (32 points to line segments) each of which is spaced apart from each other by an area filled by the deposition of said insulating film (holes are between the segments and would be filled by the dielectric 30).

Takizawa discloses that the insulating film is smoothed by chemical mechanical polishing but does not specifically disclose that the insulating film is formed by chemical vapor deposition. These limitations are "product by process" limitations. A "product by process" claim limitation is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17**(footnote 3). See also in re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116** in re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al, **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is

unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

In re claims 5 and 6, Takizawa shows (figs. 2 and 4c) that the dummy areas each have a square shape and are arranged in lattice form.

In re claim 7, Takizawa discloses that the area between each of the plurality of line patterns is approximately less than 72 microns since the dummy patterns themselves are only between 1 and 2 microns (col. 6, lines 37-38).

In re claim 8, Takizawa shows (figs. 4b or 4c) that said plurality of dummy patterns are line patterns (since each of the patterns 30 have line patterns-segments 32).

In re claim 9, Takizawa shows (figs. 1, 2, and 4b) a semiconductor device comprising: a semiconductor substrate (10) having a pattern area (containing wires 20a) and a non-pattern area (containing dummy patterns 30); a conductive pattern (20a) formed on said pattern area of said semiconductor substrate; and a plurality of dummy patterns (34) formed on said non-pattern area of said semiconductor substrate, each of said plurality of dummy patterns having a same continuous rectangular outline (see embodiment of square shape of dummy pattern in fig. 4c) as each other and being arranged in a matrix with predetermined spacing (G10); and an insulating film (40) formed on said conductive pattern and said plurality of dummy patterns, wherein the insulating film is smoothed by chemical mechanical polishing (col. 3, lines 63-67) and wherein each of said plurality of dummy patterns has an opening (32) so that a pattern

ratio of said semiconductor device is reduced (col. 4, lines 16-23). Takizawa discloses that the insulating film is smoothed by chemical mechanical polishing but does not specifically disclose that the insulating film is formed by chemical vapor deposition. These limitations are "product by process" limitations. See the explanation above for a "product by process" claim limitation.

In re claims 10 and 11, Takizawa shows (figs. 2 and 4c) that each of said plurality of dummy patterns has a square outline and that the opening has a square outline.

In re claims 12 and 13, Takizawa does not disclose the shape of the opening as being a letter or plurality of letters. However, it would have been obvious to modify the structure as disclosed by Takeuchi since applicants have presented no explanation that these particular configurations of the dummy areas are significant or are anything more than one of numerous configurations a person of ordinary skill in the art would find obvious for the purpose of providing improved integration of the interconnection layers within the semiconductor device. A change in shape is generally recognizing as being within the level of ordinary skill in the art. *In re Dailey*, 149 USPQ 47 (CCPA 1976).

In re claim 14, Takizawa shows (figs. 1, 2, and 4b) a semiconductor device comprising: a semiconductor substrate (10) having a pattern area (containing wires 20a) and a non-pattern area (containing dummy patterns 30); a conductive pattern (20a) formed on said pattern area of said semiconductor substrate; and a plurality of dummy patterns (34) formed on said non-pattern area of said semiconductor substrate, each of said plurality of dummy patterns having a same continuous rectangular outline (see

embodiment of square shape of dummy pattern in fig. 4c) as each other and being arranged in a matrix with predetermined spacing (G10); and an insulating film (40) formed on said conductive pattern and said plurality of dummy patterns, wherein the insulating film is smoothed by chemical mechanical polishing (col. 3, lines 63-67) and wherein each of said plurality of dummy patterns has an opening (32) so that a pattern ratio of said semiconductor device is reduced (col. 4, lines 16-23). Takizawa discloses that the insulating film is smoothed by chemical mechanical polishing but does not specifically disclose that the insulating film is formed by chemical vapor deposition. These limitations are "product by process" limitations. See the explanation above for a "product by process" claim limitation.

Takizawa does not disclose the shape of the opening as being a letter or plurality of letters. However, it would have been obvious to modify the structure as disclosed by Takeuchi since applicants have presented no explanation that these particular configurations of the dummy areas are significant or are anything more than one of numerous configurations a person of ordinary skill in the art would find obvious for the purpose of providing improved integration of the interconnection layers within the semiconductor device. A change in shape is generally recognizing as being within the level of ordinary skill in the art. *In re Dailey*, 149 USPQ 47 (CCPA 1976). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the opening Takizawa by forming it in the shape of a letter to improve the integration of the interconnection layers.

In re claims 15 and 16, Takizawa shows (figs. 2 and 4c) that each of said plurality of dummy patterns has a rectangular outline, an opening at the space portion, and that the opening has a square outline.

In re claims 17 and 18, Takizawa does not disclose the shape of the opening as being a letter or plurality of letters. However, it would have been obvious to modify the structure as disclosed by Takeuchi since applicants have presented no explanation that these particular configurations of the dummy areas are significant or are anything more than one of numerous configurations a person of ordinary skill in the art would find obvious for the purpose of providing improved integration of the interconnection layers within the semiconductor device. A change in shape is generally recognizing as being within the level of ordinary skill in the art. *In re Dailey*, 149 USPQ 47 (CCPA 1976).

In re claims 19 and 20, Takizawa shows (figs. 2, 4b or 4c) that said plurality of dummy patterns are line patterns (since each of the patterns 30 have line patterns (segments 32) and that each of the dummy areas has line patterns spaced apart from each other (by spacing G10). Takizawa also discloses that the line patterns are arranged with a space therebetween approximately less than 72 microns since the spacing G10 is between 1 and 2 microns (col. 3, lines 40-47).

In re claim 21, Takizawa shows (figs. 4b or 4c) that the line patterns are arranged in a same direction (since the segments on each side of the apex or center of the pattern run in the same direction).

Response to Arguments

Applicant's arguments with respect to claims 1 and 5-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew E. Warren
June 26, 2006